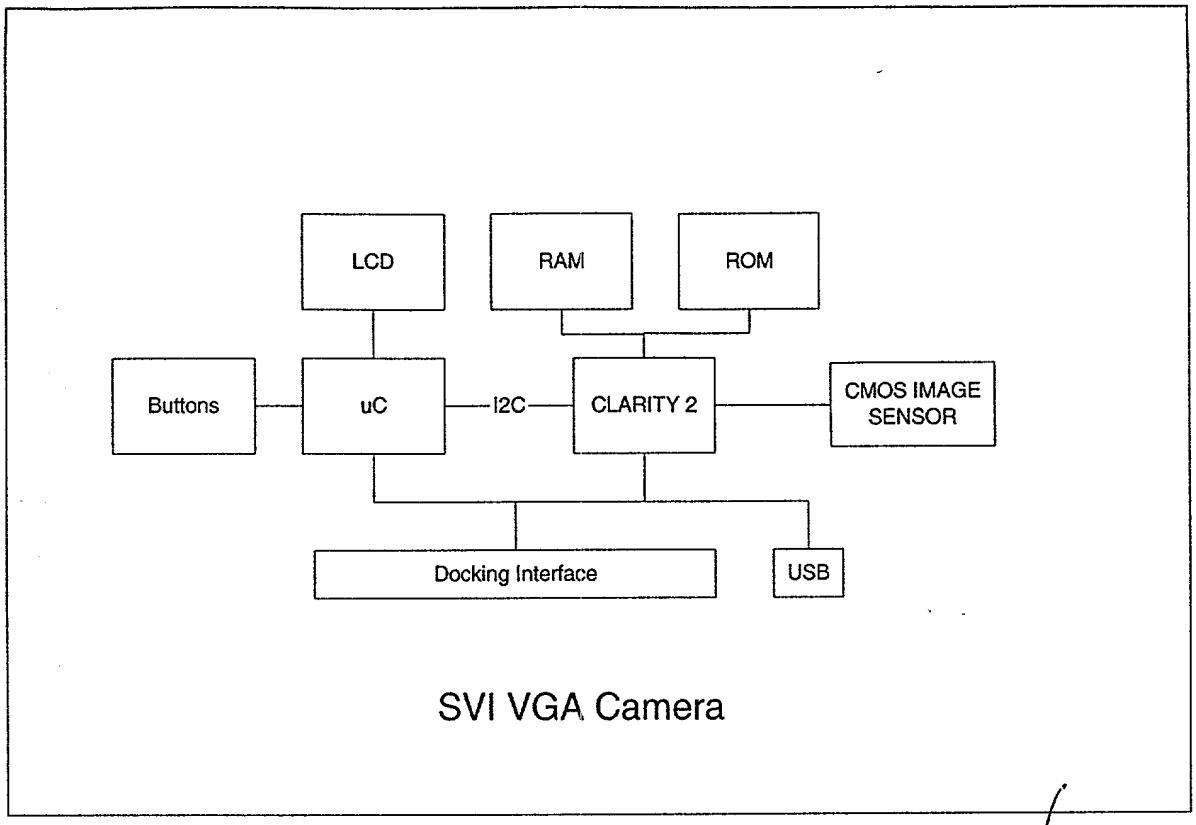
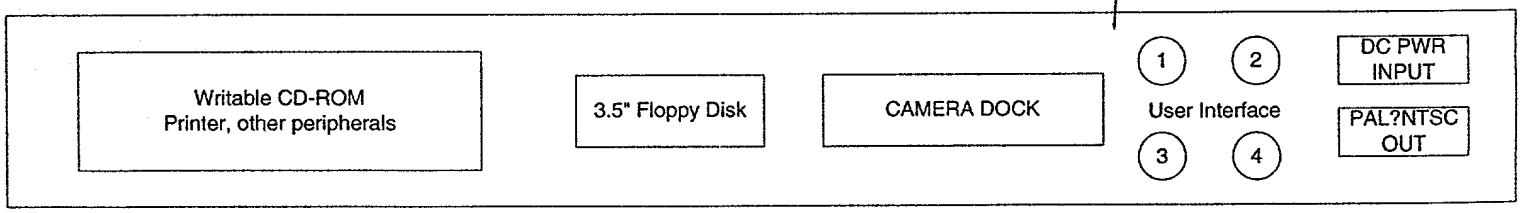


52

50

54



SVI Docking Station

FIG. 1

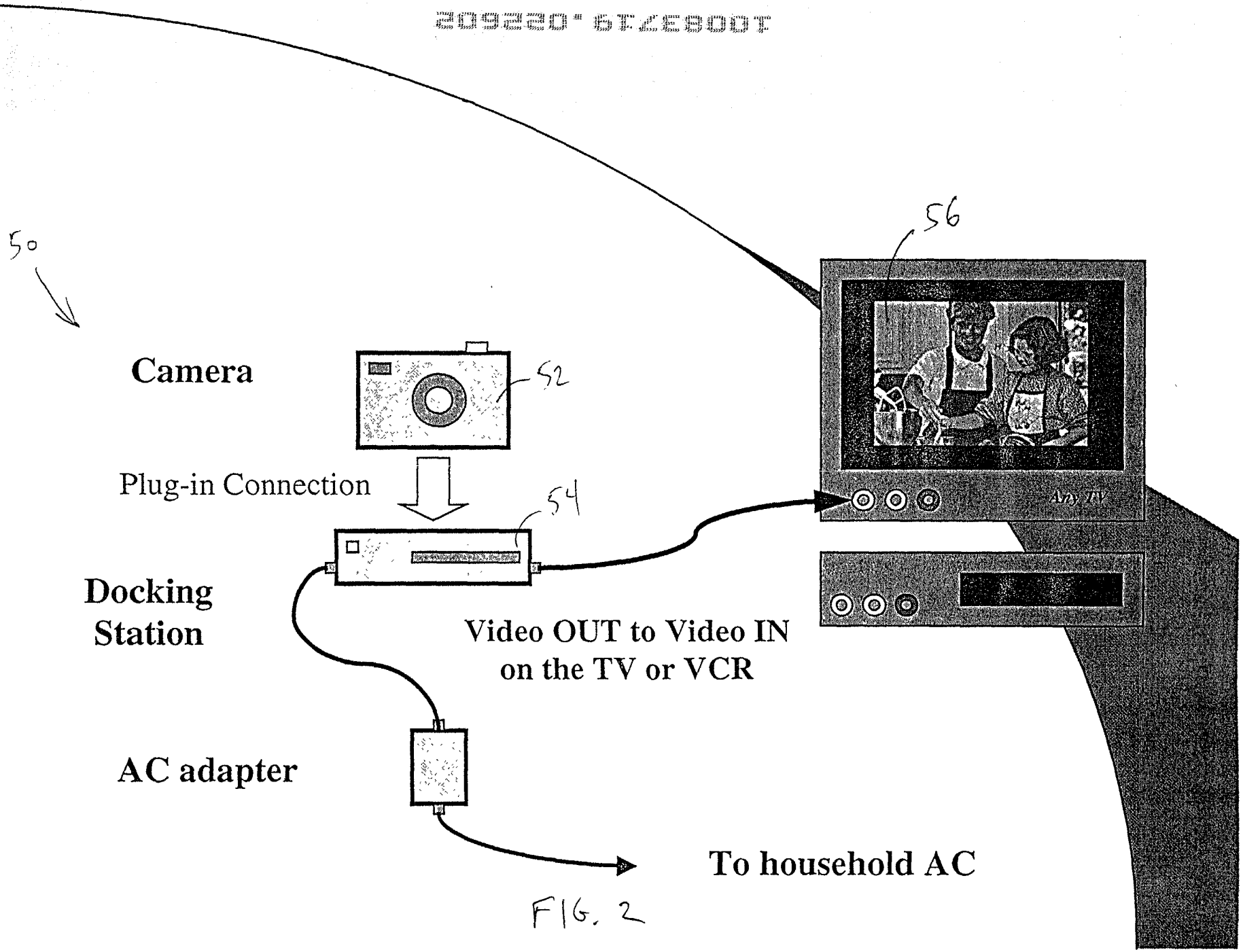


FIG. 2

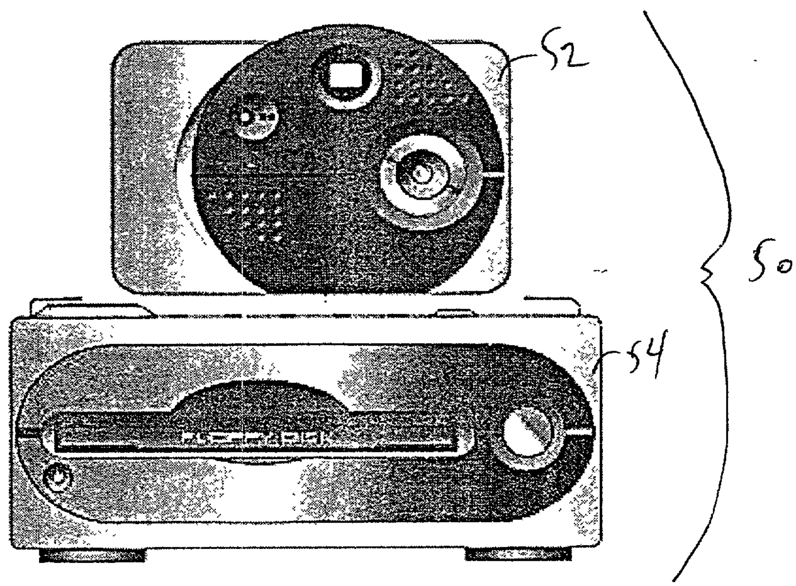


FIG. 3

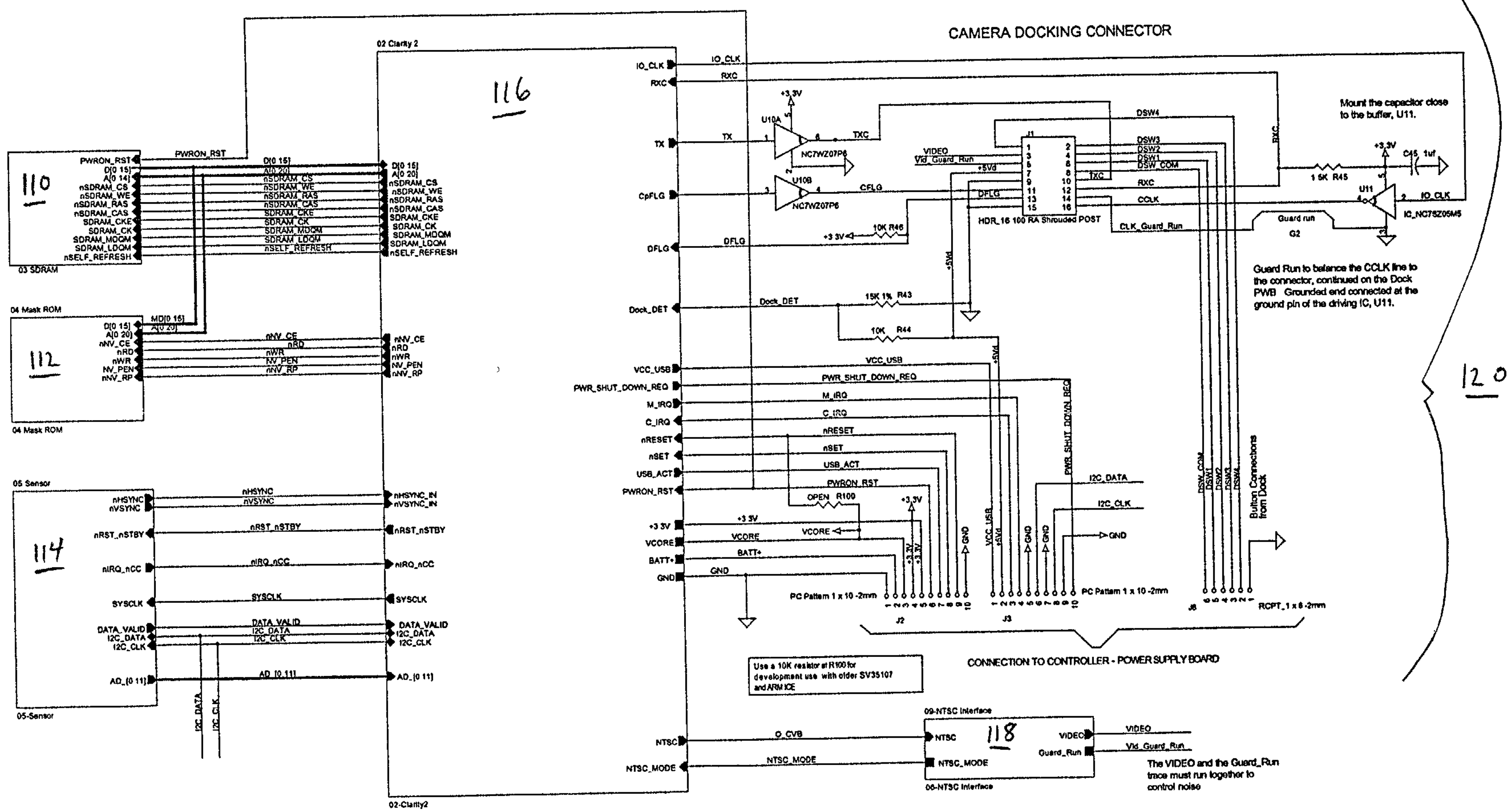
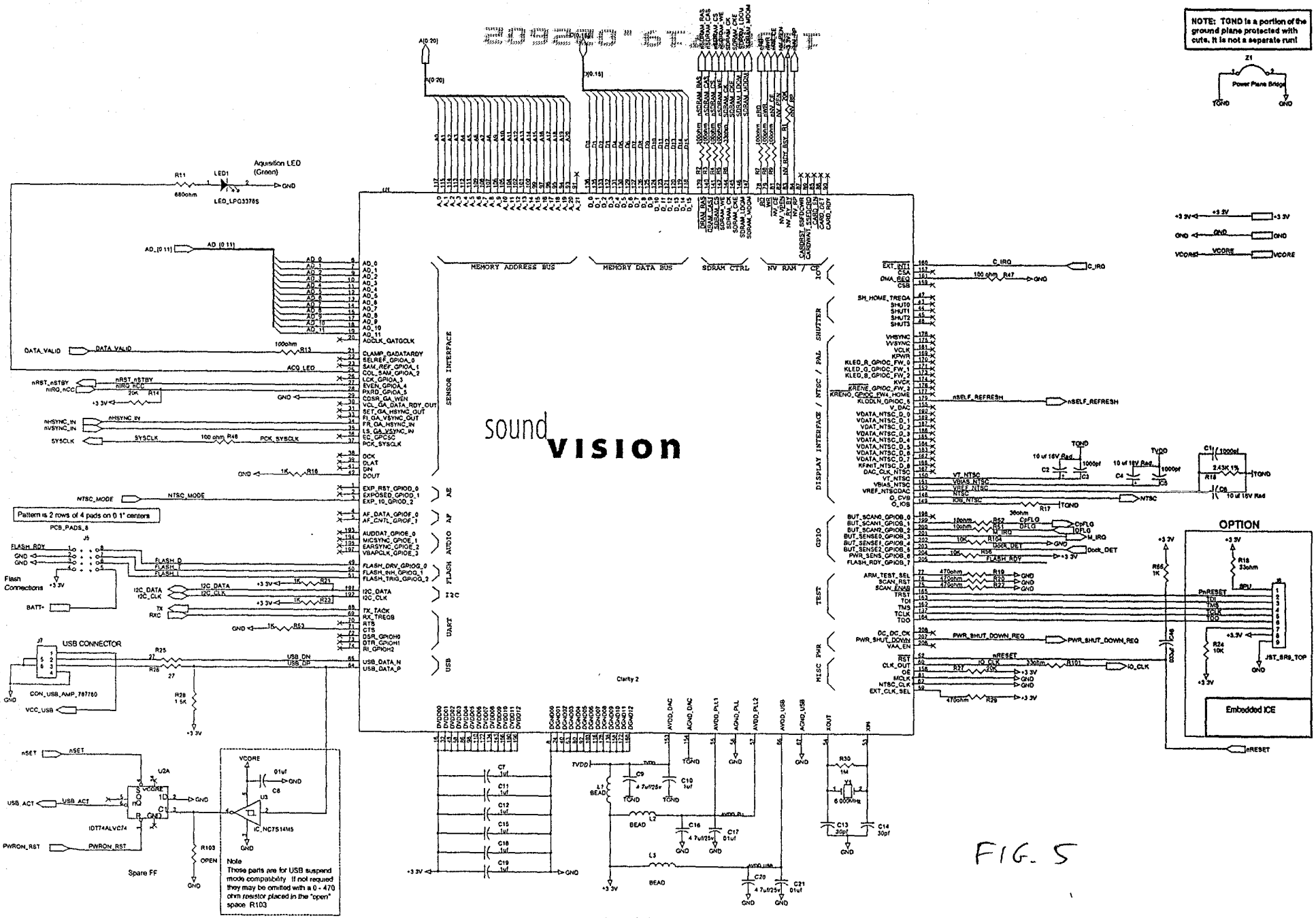
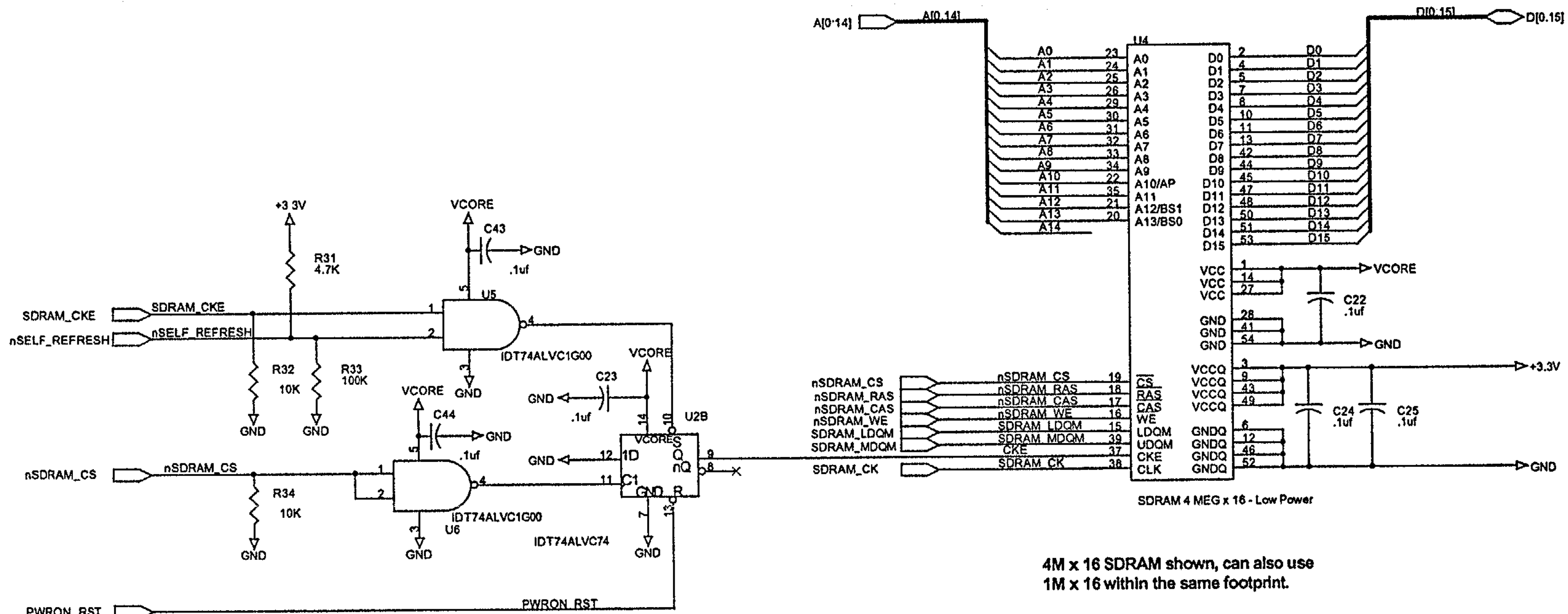

CAMERA DOCKING CONNECTOR
CONNECTION TO CONTROLLER - POWER SUPPLY BOARD
110
03 SDRAM
112
04 Mask ROM
114
05 Sensor
116
02 Clarity 2
118
09-NTSC Interface
120
Mount the capacitor close to the buffer, U11.
Guard Run to balance the CCLK line to the connector, continued on the Dock PWB Grounded end connected at the ground pin of the driving IC, U11.
Use a 10K resistor at R100 for development use with older SV35107 and ARM ICE
The VIDEO and the Guard_Run trace must run together to control noise
Button Connections from Dock
HDR_16 100 RA Shrouded POST
PC Pattern 1 x 10 -2mm
RCPT_1 x 6 -2mm

FIG. 4


NOTE: TGND is a portion of the ground plane protected with cuts. It is not a separate run!
Power Plane Bridge
TGND
GND
Aquisition LED (Green)
LED_LPG3378S
680ohm
MEMORY ADDRESS BUS
MEMORY DATA BUS
SDRAM CTRL
NV RAM / CF
SENSOR INTERFACE
NTSC / PAL SHUTTER
DISPLAY INTERFACE
GPIO
TEST
MISC PWR
AE
AF
AUDIO
FLASH
I2C
UART
USB
sound vision
Clarity 2
DATA_VALID
ACQ_LED
nRST_nSTBY
nIRQ_nCC
nHSYNC_IN
nVSYNC_IN
SYSCLK
NTSC_MODE
Pattern is 2 rows of 4 pads on 0.1" centers
PCB_PADS_8
Flash Connections
BATT+
USB CONNECTOR
CON_USB_AMP_787780
VCC_USB
nSET
USB_ACT
PWRON_RST
IDT74ALVC74
IC_NC7S14M5
Spare FF
Note
These parts are for USB suspend mode compatability. If not requied they may be omitted with a 0 - 470 ohm resistor placed in the "open" space. R103
Place the 0.1uF and 0.01uF capacitors close to the Clarity pins
OPTION
Embedded ICE
nRESET
JST_SR6_TOP
FIG. 5



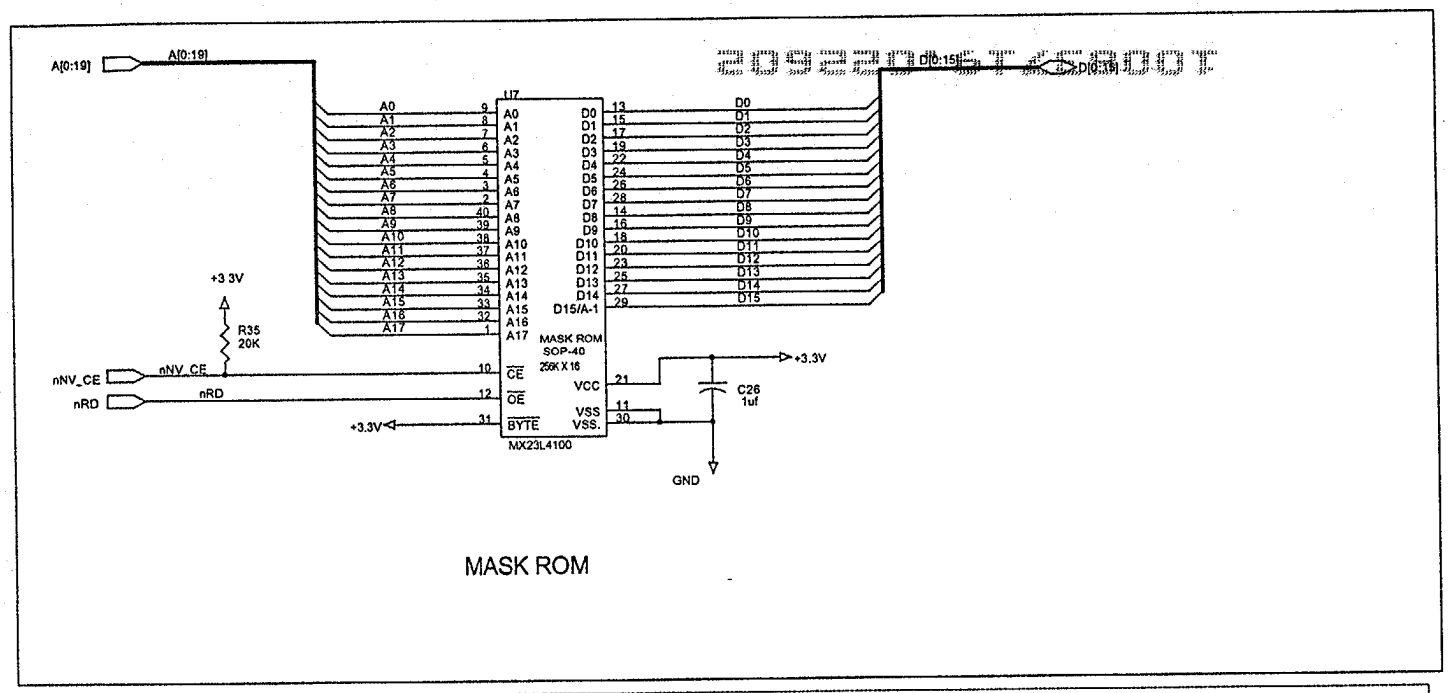
A[0:14]
A[0..14]
D[0..15]
D[0..15]
U4
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BS1 A13/BS0
D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15
VCC VCC VCC
GND GND GND
VCCQ VCCQ VCCQ VCCQ
GNDQ GNDQ GNDQ GNDQ
CS RAS CAS WE LDQM UDQM CKE CLK
VCORE
GND
+3.3V
C22 .1uf
C24 .1uf
C25 .1uf
SDRAM 4 MEG x 16 - Low Power
nSDRAM_CS
nSDRAM_RAS
nSDRAM_CAS
nSDRAM_WE
SDRAM_LDQM
SDRAM_MDQM
CKE
SDRAM_CK
SDRAM_CKE
nSELF_REFRESH
+3.3V
R31 4.7K
R32 10K
R33 100K
R34 10K
C43 .1uf
C44 .1uf
C23 .1uf
U5
U6
IDT74ALVC1G00
U2B
IDT74ALVC74
1D C1 S R Q nQ
PWRON_RST

4M x 16 SDRAM shown, can also use
1M x 16 within the same footprint.

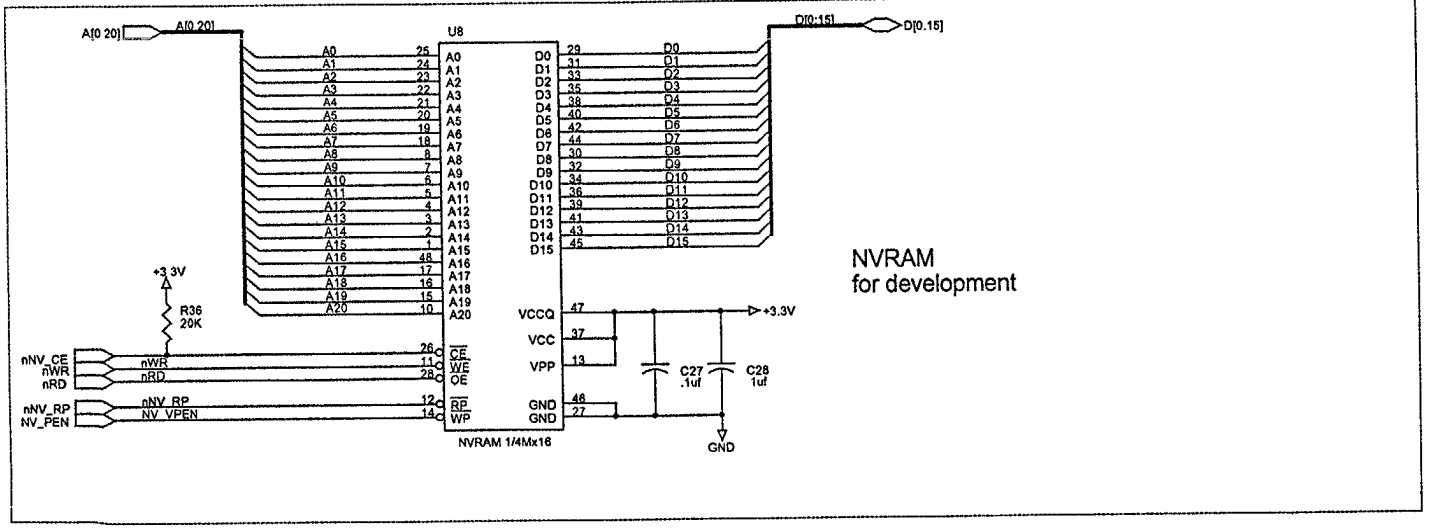
NOTE: This design requires SDRAM parts with isolated Vcc and VccQ on chip.

********** NOTE: *********
Low power SDRAM should be used. Power consumption when the camera is shut down depends on the SDRAM consumption in Self Refresh Mode as the major component of quiescent consumption.

FIG. 6



MASK ROM



NVRAM
for development

NOTES:
1. Address lines on NVRAM limited to match 160 pin Clarity 4.
2. Flash NVRAM is for prototype use only.
3. Mask ROM pinout matches similar OKI MSM534032E-SOP-40.
4. Do not duplicate the 20K resistor

FIG. 7

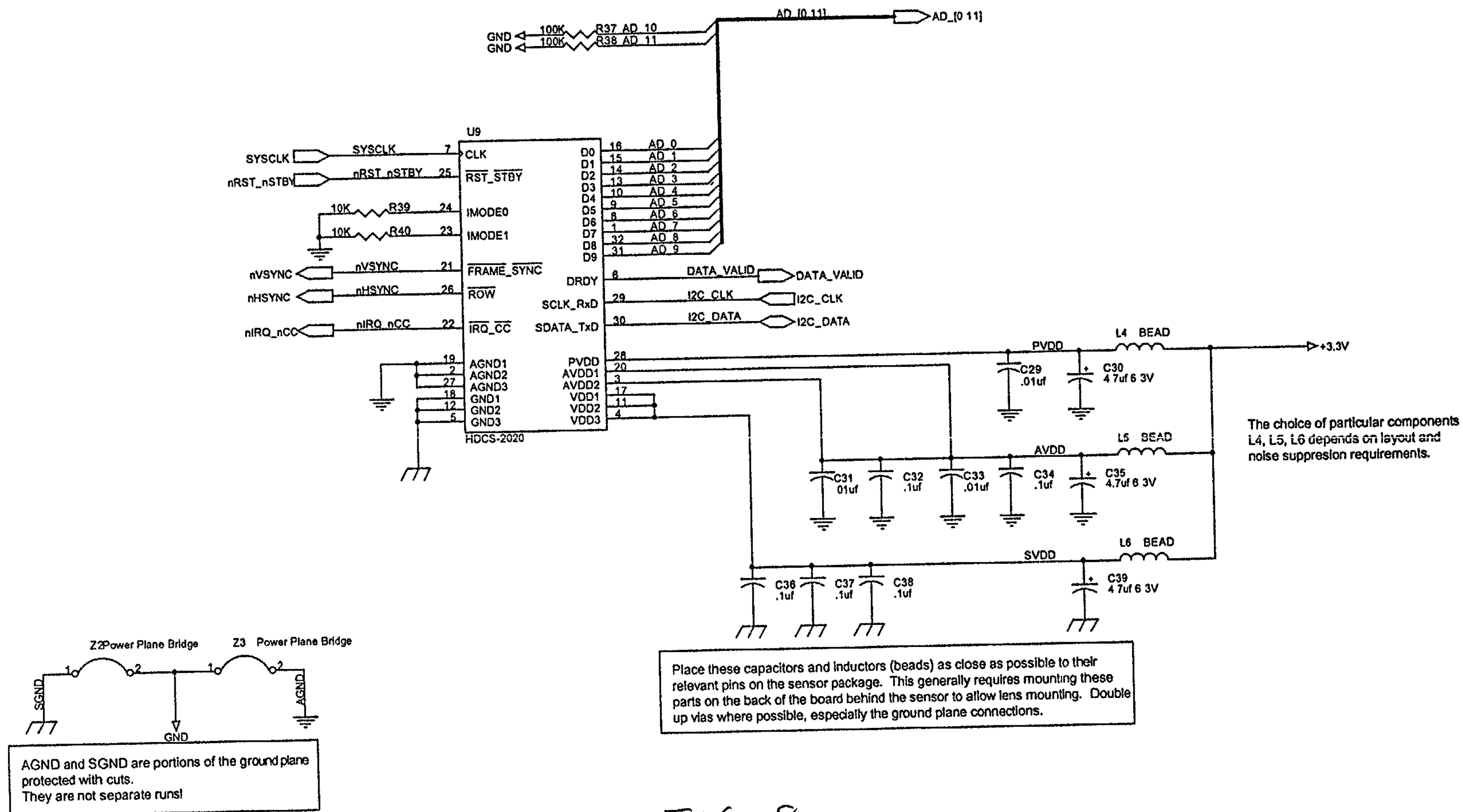
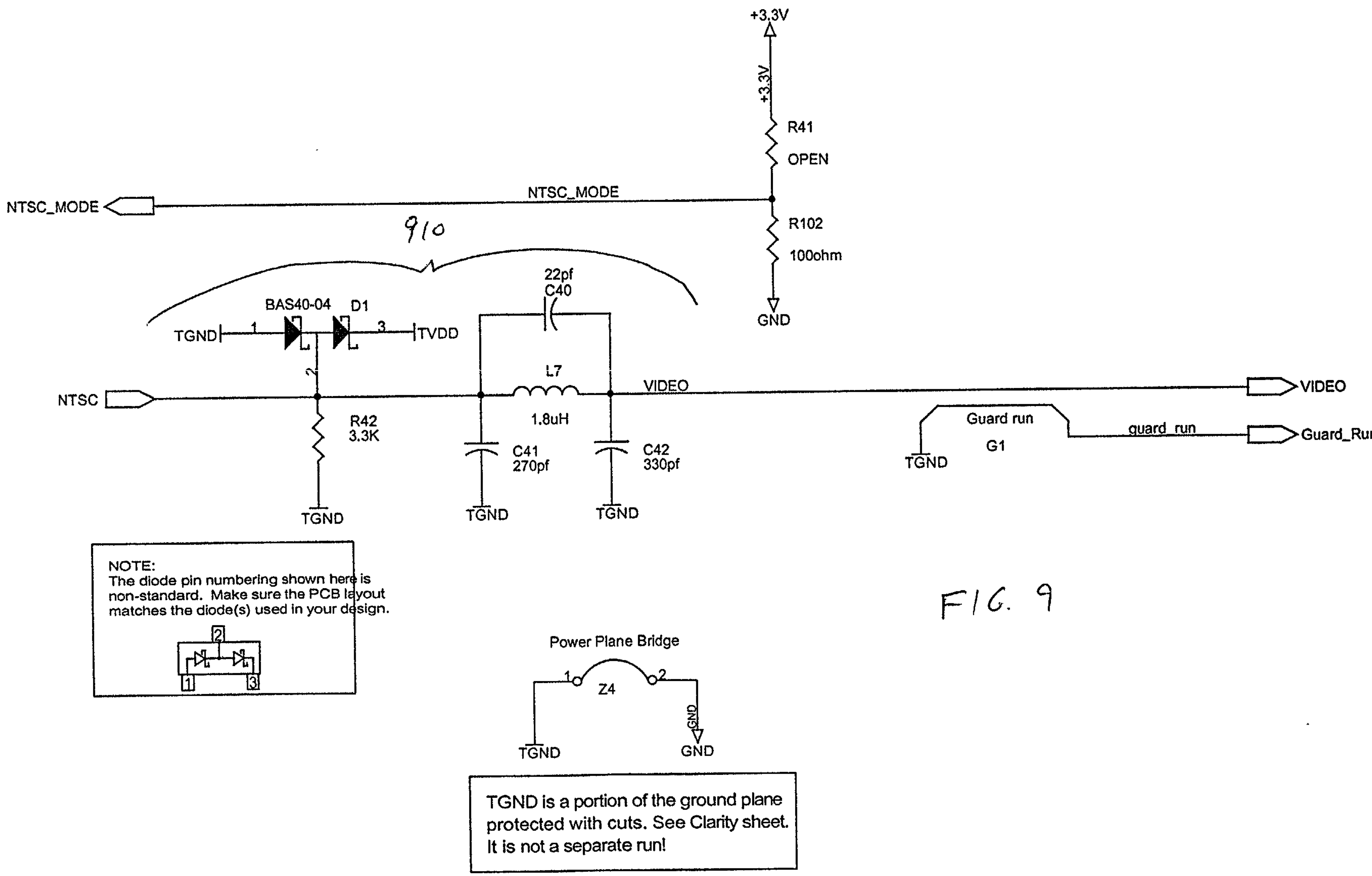

U9
HDCS-2020
CLK
RST_STBY
IMODE0
IMODE1
FRAME_SYNC
ROW
IRQ_CC
AGND1
AGND2
AGND3
GND1
GND2
GND3
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
DRDY
SCLK_RxD
SDATA_TxD
PVDD
AVDD1
AVDD2
VDD1
VDD2
VDD3
SYSCLK
nRST_nSTBY
nVSYNC
nHSYNC
nIRQ_nCC
10K R39
10K R40
GND
100K R37 AD_10
100K R38 AD_11
AD_[0 11]
AD_0
AD_1
AD_2
AD_3
AD_4
AD_5
AD_6
AD_7
AD_8
AD_9
DATA_VALID
I2C_CLK
I2C_DATA
PVDD
AVDD
SVDD
L4 BEAD
L5 BEAD
L6 BEAD
+3.3V
C29 .01uf
C30 4 7uf 6 3V
C31 .01uf
C32 .1uf
C33 .01uf
C34 .1uf
C35 4.7uf 6 3V
C36 .1uf
C37 .1uf
C38 .1uf
C39 4 7uf 6 3V
The choice of particular components L4, L5, L6 depends on layout and noise suppresion requirements.
Place these capacitors and inductors (beads) as close as possible to their relevant pins on the sensor package. This generally requires mounting these parts on the back of the board behind the sensor to allow lens mounting. Double up vias where possible, especially the ground plane connections.
Z2 Power Plane Bridge
Z3 Power Plane Bridge
SGND
AGND
GND
AGND and SGND are portions of the ground plane protected with cuts.
They are not separate runs!

FIG. 8



+3.3V
R41
OPEN
NTSC_MODE
NTSC_MODE
R102
100ohm
GND
910
BAS40-04
D1
TGND
1
3
TVDD
22pf
C40
L7
1.8uH
NTSC
VIDEO
VIDEO
R42
3.3K
C41
270pf
C42
330pf
TGND
TGND
TGND
Guard run
G1
TGND
guard_run
Guard_Run
NOTE:
The diode pin numbering shown here is non-standard. Make sure the PCB layout matches the diode(s) used in your design.
Power Plane Bridge
Z4
TGND
GND
TGND is a portion of the ground plane protected with cuts. See Clarity sheet. It is not a separate run!

FIG. 9

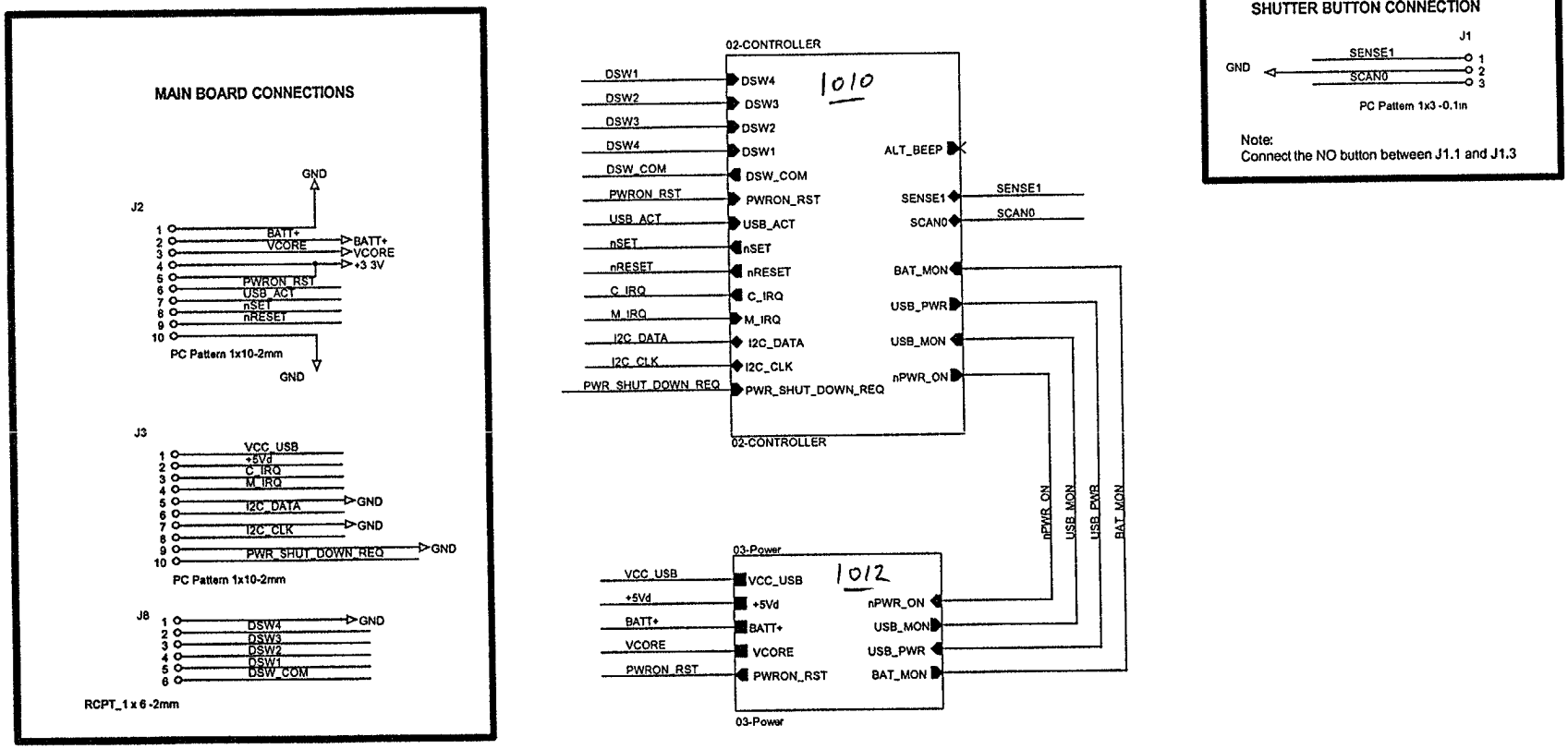


FIG. 10

NOTE:
USE VERY WIDE TRACES FOR BATT+ ,+5Vd, VCORE, VBB and the +3.3V POWER PATH, PREFERABLY ON A POWER PLANE

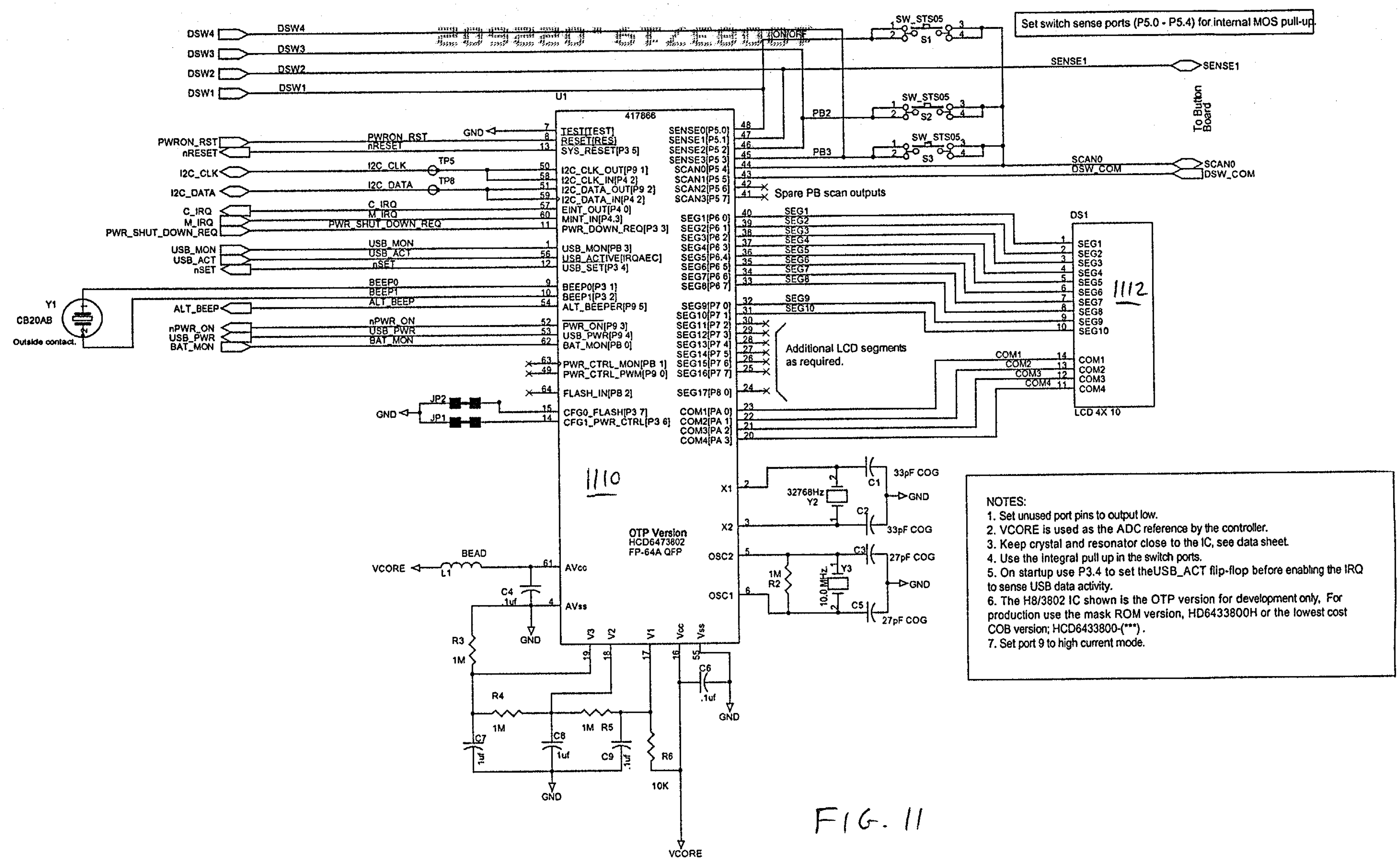

Set switch sense ports (P5.0 - P5.4) for internal MOS pull-up
DSW4
DSW3
DSW2
DSW1
SW_STS05
S1
S2
S3
SENSE1
To Button Board
PB2
PB3
SCAN0
DSW_COM
U1
417866
TEST[TEST]
RESET[RES]
SYS_RESET[P3 5]
I2C_CLK_OUT[P9 1]
I2C_CLK_IN[P4 2]
I2C_DATA_OUT[P9 2]
I2C_DATA_IN[P4 2]
EINT_OUT[P4 0]
MINT_IN[P4.3]
PWR_DOWN_REQ[P3 3]
USB_MON[PB 3]
USB_ACTIVE[IRQAEC]
USB_SET[P3 4]
BEEP0[P3 1]
BEEP1[P3 2]
ALT_BEEPER[P9 5]
PWR_ON[P9 3]
USB_PWR[P9 4]
BAT_MON[PB 0]
PWR_CTRL_MON[PB 1]
PWR_CTRL_PWM[P9 0]
FLASH_IN[PB 2]
CFG0_FLASH[P3 7]
CFG1_PWR_CTRL[P3 6]
SENSE0[P5.0]
SENSE1[P5.1]
SENSE2[P5 2]
SENSE3[P5 3]
SCAN0[P5 4]
SCAN1[P5 5]
SCAN2[P5 6]
SCAN3[P5 7]
Spare PB scan outputs
SEG1[P6 0] … SEG8[P6 7]
SEG9[P7 0] … SEG16[P7 7]
SEG17[P8 0]
COM1[PA 0]
COM2[PA 1]
COM3[PA 2]
COM4[PA 3]
Additional LCD segments as required.
DS1
LCD 4X 10
1112
1110
OTP Version
HCD6473802
FP-64A QFP
PWRON_RST
nRESET
I2C_CLK
I2C_DATA
TP5
TP8
C_IRQ
M_IRQ
PWR_SHUT_DOWN_REQ
USB_MON
USB_ACT
nSET
BEEP0
BEEP1
ALT_BEEP
nPWR_ON
USB_PWR
BAT_MON
Y1
CB20AB
Outside contact.
GND
JP1
JP2
VCORE
BEAD
L1
C4 .1uf
AVcc
AVss
X1
X2
OSC2
OSC1
32768Hz Y2
33pF COG
27pF COG
10.0 MHz Y3
1M R2
R3 1M
R4 1M
1M R5
R6 10K
C6 .1uf
C7 1uf
C8 1uf
C9 .1uf
NOTES:
1. Set unused port pins to output low.
2. VCORE is used as the ADC reference by the controller.
3. Keep crystal and resonator close to the IC, see data sheet.
4. Use the integral pull up in the switch ports.
5. On startup use P3.4 to set theUSB_ACT flip-flop before enabling the IRQ to sense USB data activity.
6. The H8/3802 IC shown is the OTP version for development only, For production use the mask ROM version, HD6433800H or the lowest cost COB version; HCD6433800-(***).
7. Set port 9 to high current mode.

FIG. 11

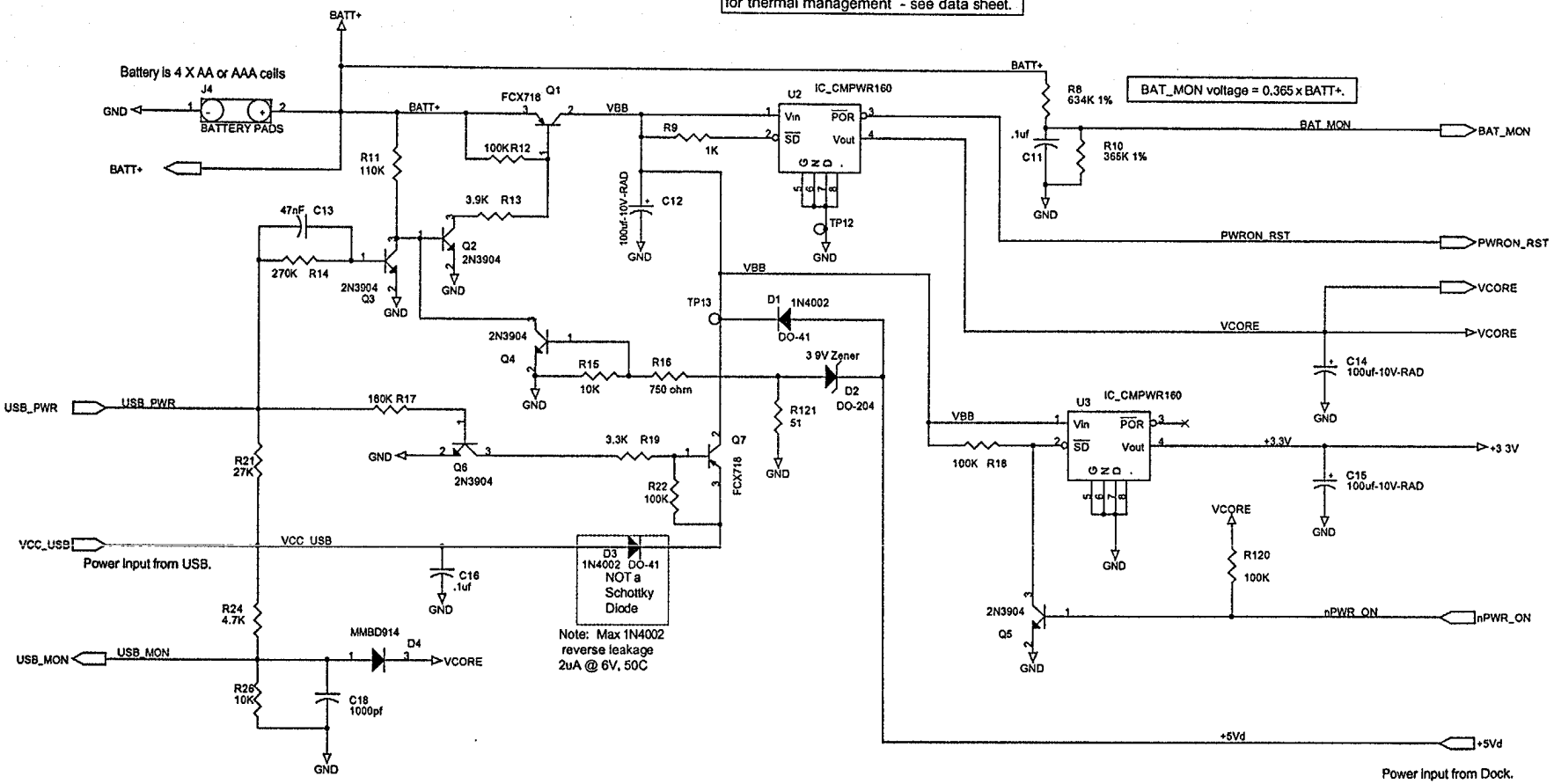


FIG. 12

NOTE:
USE VERY WIDE TRACES FOR BATT+ ,+5Vd, VCORE, VBB and the +3.3V POWER PATH, PREFERABLY ON A POWER PLANE

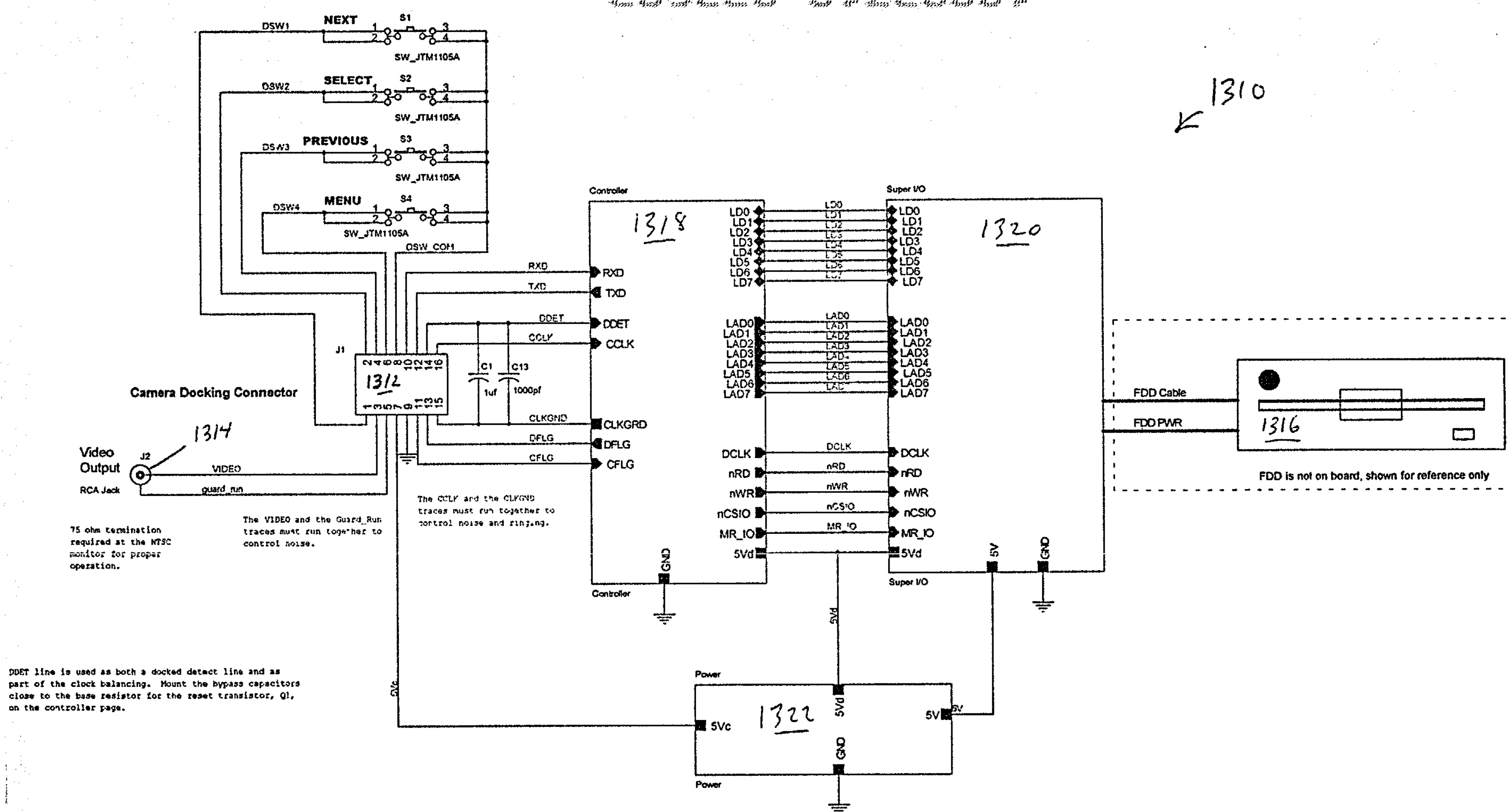

1310
NEXT
SELECT
PREVIOUS
MENU
S1
S2
S3
S4
SW_JTM1105A
DSW1
DSW2
DSW3
DSW4
DSW_COM
Camera Docking Connector
J1
1312
1314
Video Output
J2
RCA Jack
VIDEO
guard_run
C1
1uf
C13
1000pf
RXD
TXD
DDET
CCLK
CLKGND
DFLG
CFLG
Controller
1318
CLKGRD
GND
LD0
LD1
LD2
LD3
LD4
LD5
LD6
LD7
LAD0
LAD1
LAD2
LAD3
LAD4
LAD5
LAD6
LAD7
DCLK
nRD
nWR
nCSIO
MR_IO
5Vd
Super I/O
1320
5V
FDD Cable
FDD PWR
1316
FDD is not on board, shown for reference only
Power
1322
5Vc
75 ohm termination required at the NTSC monitor for proper operation.
The VIDEO and the Guard_Run traces must run together to control noise.
The CCLK and the CLKGND traces must run together to control noise and ringing.
DDET line is used as both a docked detect line and as part of the clock balancing. Mount the bypass capacitors close to the base resistor for the reset transistor, Q1, on the controller page.

FIG. 13

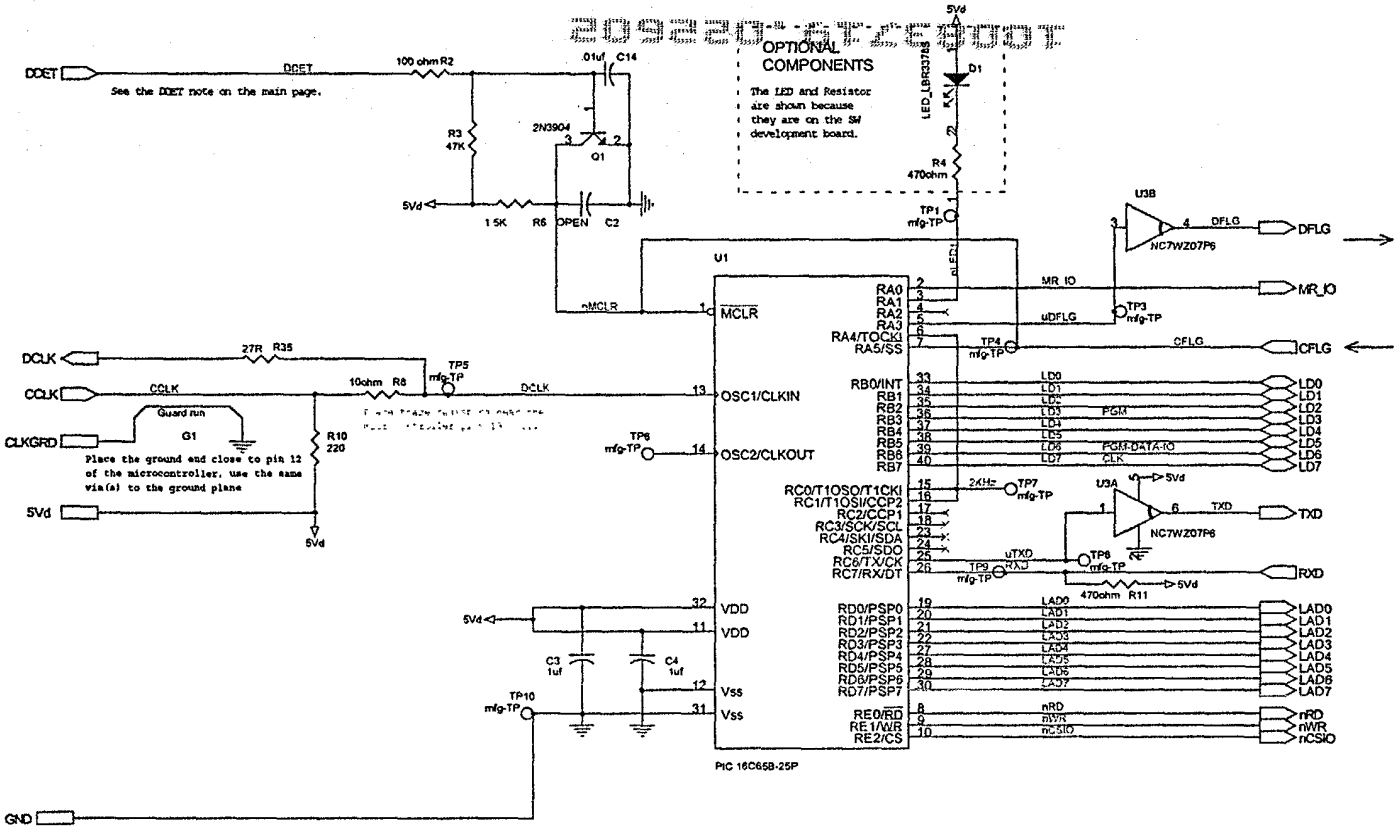
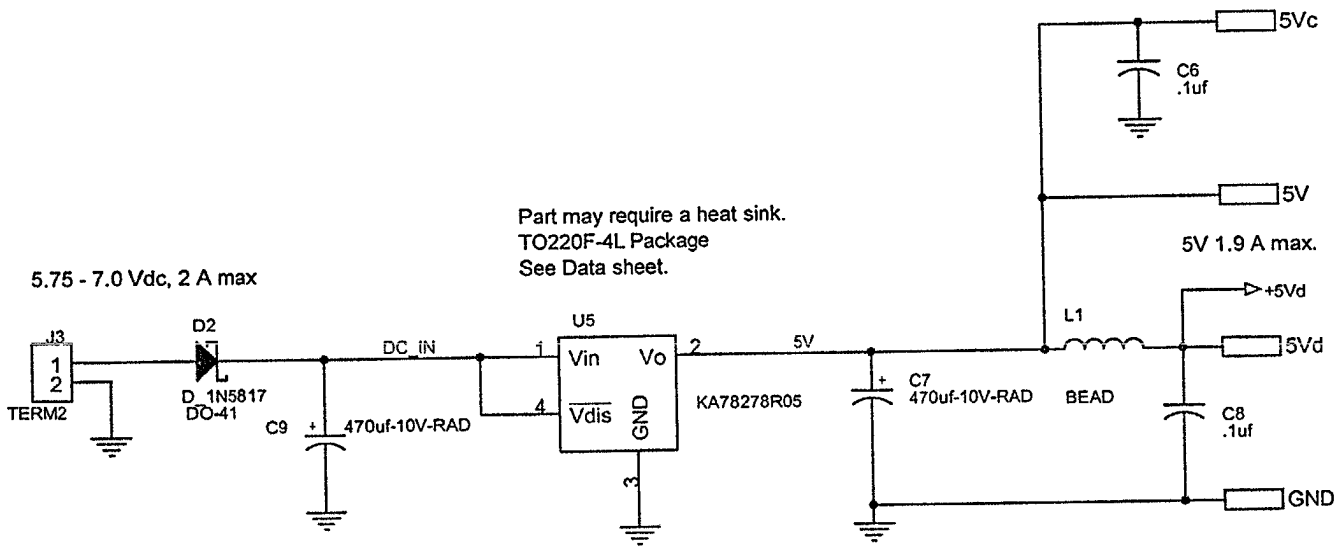

DDET
100 ohm R2
.01uf C14
See the DDET note on the main page.
OPTIONAL COMPONENTS
The LED and Resistor are shown because they are on the SM development board.
LED_LBR33788
D1
R4 470ohm
5Vd
R3 47K
2N3904
Q1
1.5K R6
OPEN C2
TP1 mfg-TP
U3B
NC7WZ07P6
DFLG
MR_IO
uDFLG
TP3 mfg-TP
CFLG
TP4 mfg-TP
U1
nMCLR
MCLR
RA0
RA1
RA2
RA3
RA4/T0CKI
RA5/SS
DCLK
27R R35
TP5 mfg-TP
CCLK
10ohm R8
Guard run
G1
CLKGRD
Place the ground end close to pin 12 of the microcontroller, use the same via(s) to the ground plane
R10 220
OSC1/CLKIN
OSC2/CLKOUT
TP6 mfg-TP
RB0/INT
RB1
RB2
RB3
RB4
RB5
RB6
RB7
LD0
LD1
LD2
LD3
LD4
LD5
LD6
LD7
PGM
PGM-DATA-IO
CLK
RC0/T1OSO/T1CKI
RC1/T1OSI/CCP2
RC2/CCP1
RC3/SCK/SCL
RC4/SDI/SDA
RC5/SDO
RC6/TX/CK
RC7/RX/DT
2KHz
TP7 mfg-TP
U3A
TXD
uTXD
TP8 mfg-TP
TP9 mfg-TP
RXD
470ohm R11
VDD
VDD
Vss
Vss
C3 1uf
C4 1uf
TP10 mfg-TP
RD0/PSP0
RD1/PSP1
RD2/PSP2
RD3/PSP3
RD4/PSP4
RD5/PSP5
RD6/PSP6
RD7/PSP7
LAD0
LAD1
LAD2
LAD3
LAD4
LAD5
LAD6
LAD7
RE0/RD
RE1/WR
RE2/CS
nRD
nWR
nCSIO
PIC 16C65B-25P
GND

FIG. 14



Note power supply is to be sized for the particular floppy disk drive's maximum load, allow ~300 mA for other loads.

Sizing affects choice of U5 and its heatsink, the filter capacitors, C7, C9 and the AC adapter rating.

FIG. 15

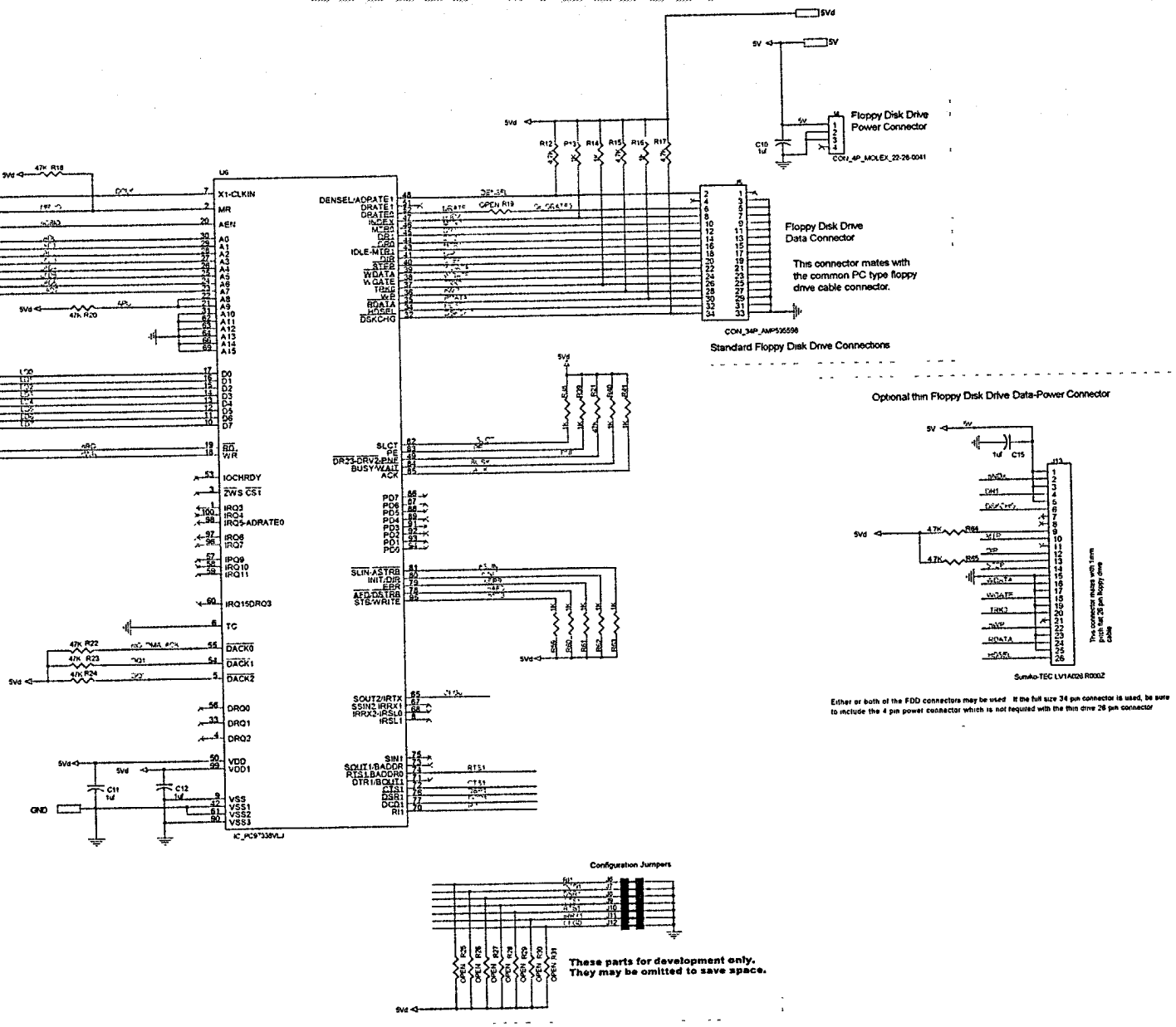


FIG. 16